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ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 06/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)
Office Action Summary		10/768,441	NAMBU ET AL.
		Examiner	Art Unit
		James Sugent	2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on <u>02 February 2004</u>.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) <u>1-10</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) <u>1-10</u> is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>February 2, 2004</u>.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

The information disclosure statement (IDS) submitted on February 2, 2004 was filed. The

5   submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information

disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

10   basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless —

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed
in the United States before the invention by the applicant for patent or (2) a patent granted on an application for
patent by another filed in the United States before the invention by the applicant for patent, except that an
15   international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this
subsection of an application filed in the United States only if the international application designated the United
States and was published under Article 21(2) of such treaty in the English language.

Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Coteus et al.

20   (U.S. Patent No. 6,807,125 B2) (hereinafter referred to as Coteus).

As to claim 1, Coteus discloses a semiconductor integrated circuit comprising: a clock

input terminal (13) for receiving a clock signal (DQS) and a data input terminal (12) for

receiving a data signal (DQ) (column 2, lines 22-26); an internal clock generating circuit (19) for

generating an internal clock signal (DQS_CLK and DQSN_CLK) which is switched at an

25   intermediate timing between the i-th (i: an integer of 1 or larger) switch timing and the (i+1)th

switch timing of the clock signal input to said clock input terminal (as shown in figure 3) (Coteus

discloses the internal clock generated [DQS_CLK] switches at an intermediate timing between

the (i+1)th interval [90° out of phase]; column 2, lines 37-62); and a latch circuit (21 and 22) for

latching the data signal input (DQ) to said data input terminal synchronously with said internal

clock signal (Coteus discloses the incoming data being input into latches [21 and 22] are

synchronized with the internal clocks [DQS_CLK and DQSN_CLK] as latch enable signals

5   CLKS; column 2, lines 54-62).

As to claim 2, Coteus discloses the semiconductor integrated circuit wherein said internal

clock generating circuit includes: first means (60) for holding a delay amount (DELAY_STEPS)

corresponding to time which is the half of the difference between the (i-j)th switch timing and

the (i+1+j)th (j: an integer of 0 or larger) switch timing of the clock signal (an amount

10   corresponding to switching of (2j+1) times) (Coteus discloses components 60 and 66 of the

internal clock generating circuit [19] delaying the input clock [DQS] at a variable amount and

therefore any fraction of said input clock DQS; column 4, line 54 thru column 6, line 10); and

second means (66) for generating said internal clock by delaying said clock signal only by time

of said held delay amount (column 4, line 54 thru column 6, line 10).

15

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

20   (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
          section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
          such that the subject matter as a whole would have been obvious at the time the invention was made to a person
          having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
          manner in which the invention was made.

25   Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus et

al. (U.S. Patent No. 6,807,125 B2) (hereinafter referred to as Coteus) as applied to claim 1

above, and further in view of Kawasaki et al. (U.S. Patent No. 6,066,969) (hereinafter referred to as Kawasaki).

As to claim 3, Coteus fails to disclose the semiconductor integrated circuit wherein said internal clock generating circuit is constructed by first and second frequency dividers, a phase

5   comparator, a variable delay circuit, and a delay control circuit and comprises: the first frequency divider for generating a first frequency divided signal synchronized with the (i-j)th switch timing of said clock signal; the second frequency divider for generating a second frequency divided signal synchronized with the (i+1+j)th switch timing of said clock signal; the phase comparator for comparing the phase of said first frequency divided signal and the phase of said second

10   frequency divided signal; and the delay control circuit for controlling said variable delay circuit so as to have delay time corresponding to time which is the half of said phase difference, wherein said clock signal is input to the variable delay circuit, and an output signal of the variable delay circuit is used as said internal clock signal.

Kawasaki teaches a clock generating circuit [DLL figure 3] wherein said clock generating

15   circuit is constructed by first (32) and second (31) frequency dividers, a phase comparator (33), a variable delay circuit (12), and a delay control circuit (18) and comprises: the first frequency divider (32) for generating a first frequency divided signal (dll-clk-div) (column 8, lines 50-59 and column 9, lines 23-35); the second frequency divider (31) for generating a second frequency divided signal (i-clk-div) (column 8, lines 50-59 and column 9, lines 23-35); the phase

20   comparator (33) for comparing the phase of said first frequency divided signal (dll-clk-div) and the phase of said second frequency divided signal (i-clk-div) (column 8, lines 50-59); and the delay control circuit (18) for controlling said variable delay circuit (12) so as to have a variable

delay time (Kawasaki discloses the delay control circuit setting a variable delay time dependent

on the results of the phase comparator circuit [17]; column 7, lines 9-17 and column 7, lines 43-

55), wherein said clock signal (i-clk) is input to the variable delay circuit (12), and an output

signal of the variable delay circuit (dll-clk) is used as said internal clock signal (column 6, lines

5   37-41). Kawasaki also has the added feature of reducing excessive power consumption and

shorten a time period required for achieving a lock-on condition when a clock signal switches

from a longer cycle to a shorter cycle (column 3, lines 50-55).

It would have been obvious to one of ordinary skill of the art having the teachings of

Coteus and Kawasaki at the time the invention was made, to modify the clock generating circuit

10   of Coteus to include the DLL components as taught by Kawasaki such that the first frequency

divider is synchronized with the (i-j)th switch timing of said clock signal, the second frequency

divider is synchronized with the (i+1+j)th switch timing of said clock signal and the delay clock

circuit has a delay time corresponding to time which is the half of said phase different. One of

ordinary skill in the art would be motivated to make this combination altering the clock

15   generating circuit to include the DLL componenets in view of the teachings of Kawasaki, as

doing so would give the added benefit of reducing excessive power consumption and shorten a

time period required for achieving a lock-on condition when a clock signal switches from a

longer cycle to a shorter cycle (column 3, lines 50-55).

As to claim 4, Kawasaki teaches the semiconductor integrated circuit further comprising

20   a clock input buffer (11) for receiving a clock signal which is input to said clock input terminal,

wherein said clock input buffer (in combination with the variable delay circuit 12) generates a

first clock signal (dll-clk) and a second clock signal (i-clk) at a level complementary to the first

clock signal (which can variably also be an inversion of the input clk), wherein, when the first

clock signal (dll-clk) is input to said first frequency divider (32), the second clock signal (i-clk)

is input to said second frequency divider (31), and wherein, when the first clock signal (dll-clk)

is input to said second frequency divider (31), the second clock signal i-clk) is input to said first

5   frequency divider (32) (column 8, lines 50-67).

Claims 5-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coteus et al.

(U.S. Patent No. 6,807,125 B2) (hereinafter referred to as Coteus) in view of Kawasaki et al.

(U.S. Patent No. 6,066,969) (hereinafter referred to as Kawasaki) and Fujieda et al. (U.S. Patent

No. 6,181,174 B1) (hereinafter referred to as Fujieda).

10   As to claim 5, Coteus discloses a semiconductor integrated circuit comprising: a clock

input terminal (13); a data input terminal (12); an internal clock generating circuit (19) for

generating an internal clock signal (DQS_CLK and DQSN_CLK) from a clock signal (DQS)

which is input to said clock input terminal (column 2, lines 37-62); and a latch circuit (21 and

22) for latching a data signal input (DQ) to said data input terminal synchronously with said

15   internal clock signal (Coteus discloses the incoming data being input into latches [21 and 22] are

synchronized with the internal clocks [DQS_CLK and DQSN_CLK] as latch enable signals

CLKS; column 2, lines 54-62).

Coteus fails to disclose said internal clock generating circuit includes: a first variable

delay circuit for receiving said clock signal and outputting said internal clock signal; a second

20   variable delay circuit for delaying said clock signal or an inversion signal of said clock signal; a

third variable delay circuit for delaying an output signal of said second variable delay circuit; a

first frequency divider for dividing frequency of an output signal of said third variable delay

circuit; a second frequency divider for dividing frequency of said clock signal or the inversion

signal of said clock signal; a phase comparator for comparing phase of a first frequency divided

signal output from the first frequency divider with phase of a second frequency divided signal

output from the second frequency divider; and a delay control circuit for outputting a delay

5   control signal for controlling said first, second, and third variable delay circuits on the basis of an

output signal of said phase comparator, wherein said first, second, and third variable delay

circuits have the same configuration, wherein said first frequency divider generates a first

frequency divided signal synchronized with the (i-j)th switch timing of said clock signal (where i

denotes an integer of 1 or larger and j denotes an integer of 0 or larger), wherein said second

10   frequency divider generates a second frequency divided signal synchronized with the (i+1+j)th

switch timing of said clock signal, wherein said phase comparator compares the phase of said

first frequency divided signal with the phase of said second frequency divided signal to obtain a

phase difference, and wherein said delay control circuit controls delay times of said first, second,

and third variable delay circuits so that said phase difference becomes zero.

15   Kawasaki teaches disclose said internal clock generating circuit includes: a first variable

delay circuit (12) for receiving a clock signal (i-clk) and outputting said internal clock signal

(dll-clk) (column 6, lines 37-41); a second variable delay circuit (19) for delaying a divided clock

of the input clock (i-clk) (column 6, lines 57-62); a third dummy delay circuit (21) for delaying

an output signal of said second variable delay circuit (Kawasaki teaches a third delay circuit [21]

20   receiving, via clock control circuit 20, the delayed clock from a second variable delay circuit

[19]; column 6, line 62 thru column 7, line 1); a first frequency divider (32) for dividing

frequency of an output signal of said third delay circuit (Kawasaki teaches a first frequency

divider [32] the divides an indirect output signal from a dummy delay circuit [21] via circuit

elements 22, 23, 24, 17, 18 and 12; column 6, line 57 thru column 7, line 17 and column 8, lines

50-59); a second frequency divider (31) for dividing frequency of said clock signal (i-clk) or the

inversion signal of said clock signal (column 8, lines 50-59); a phase comparator (33) for

5   comparing phase of a first frequency divided signal (dll-clk-div) output from the first frequency

divider (32) with phase of a second frequency divided signal (i-clk-div) output from the second

frequency divider (32) (column 8, lines 60-67); and a delay control circuit (18) for outputting a

delay control signal for controlling said first (12) and second (19) variable delay circuits on the

basis of an output signal of said phase comparator (Kawasaki discloses the output signal [CKS]

10   from the phase comparator [33] indirectly controls, via a second phase comparator [17], the

control signal from the delay control circuit [18] for delay circuits 12 and 19; column 7, lines 9-

17 and column 7, lines 31-55), wherein said first and second variable delay circuits (12 and 19)

have the same configuration (figure 10), wherein said phase comparator (33) compares the phase

of said first frequency divided signal (dll-clk-div) with the phase of said second frequency

15   divided signal (i-clk-div) (column 8, lines 50-59). Kawasaki also has the added feature of

reducing excessive power consumption and shorten a time period required for achieving a lock-

on condition when a clock signal switches from a longer cycle to a shorter cycle (column 3, lines

50-55).

        It would have been obvious to one of ordinary skill of the art having the teachings of

20   Coteus and Kawasaki at the time the invention was made, to modify the clock generating circuit

of Coteus to include the DLL components as taught by Kawasaki such that the first frequency

divider is synchronized with the (i-j)th switch timing of said clock signal, the second frequency

divider is synchronized with the (i+1+j)th switch timing of said clock signal, the delay clock

circuit has a delay time corresponding to time which is the half of said phase different, the

second variable delay circuit delays the input clock signal or an inversion of said clock signal

and . One of ordinary skill in the art would be motivated to make this combination altering the

5   clock generating circuit to include the DLL componenets in view of the teachings of Kawasaki,

as doing so would give the added benefit of reducing excessive power consumption and shorten

a time period required for achieving a lock-on condition when a clock signal switches from a

longer cycle to a shorter cycle (column 3, lines 50-55).

Neither Coteus nor Kawasaki teaches the third delay circuit is a variable delay circuit

10   wherein said third delay circuit also has the same configuration as the first and second variable

delay circuits. Coteus and Kawasaki also fail to teach the phase comparator obtaining a phase

difference and that said delay control circuit controls delays of the first, second and third variable

circuits so that said phase difference becomes zero.

Fujieda teaches another internal semiconductor DLL that comprises three variable delay

15   circuits (41, 42 and 45) that all have the same configuration and are all controlled by the delay

control circuit (47) (column 6, lines 10-16 and column 9, lines 16-24). Fujieda further teaches a

phase comparator (44) that measures the phase difference between two different divided clock

signals (X and Z), delivers a resultant phase difference signal to the delay control circuit (47) to

ensure that the variable delay times of the first, second and third variable delay signals have a

20   zero phase difference (column 5, line 61 thru column 6, line 10). Fujieda also has the added

feature of providing the semiconductor device does not cause an underflow and an overflow of a

DLL circuit even if the frequency of the internal clock becomes high or low (column 2, lines 35-41).

It would have been obvious to one of ordinary skill of the art having the teachings of Coteus, Kawasaki and Fujieda at the time the invention was made, to modify the clock

5   generating circuit of Coteus and Kawasaki to include the addition features as taught by Fujieda such that the third delay circuit is a variable delay circuit wherein said third delay circuit also has the same configuration as the first and second variable delay circuits and the phase comparator obtaining a phase difference and that said delay control circuit controls delays of the first, second and third variable circuits so that said phase difference becomes zero. One of ordinary skill in the

10   art would be motivated to make this combination of including the additional DLL features in view of the teachings of Fujieda, as doing so would give the added feature of providing the semiconductor device does not cause an underflow and an overflow of a DLL circuit even if the frequency of the internal clock becomes high or low (column 2, lines 35-41).

As to claim 6, Fujieda teaches the semiconductor integrated circuit wherein each of said

15   first and second frequency dividers (36 and 38) is constructed by connecting a plurality of latch circuits in series and, by setting initial states of the latch circuits, the value of j is set (As shown in figure 6; column 7, lines 29-44).

As to claim 7, Kawasaki teaches the semiconductor integrated circuit wherein the initial state of said latch circuit can be set by a fuse signal or an external input signal (Providing a

20   predetermined timing relation dependent on the CLK signal which is an external input signal; column 6, lines 46-56).

As to claim 8, Fujieda teaches the semiconductor integrated circuit wherein a dummy

delay circuit (45) having delay time which is twice as long as time obtained by subtracting delay

time of a signal transmitted from said data input terminal to said latch circuit from the sum of

delay time of a signal transmitted from said clock input terminal to the first variable delay circuit

5   and delay time of a signal transmitted from the first variable delay circuit to said latch circuit is

disposed in some midpoint of a signal path extending from said clock input terminal to the first

frequency divider (column 5, line 61 thru column 6, line 10).

As to claim 9, Coteus discloses a semiconductor integrated circuit comprising: a clock

input terminal (13); a data input terminal (12); an internal clock generating circuit (19) for

10   generating an internal clock signal (DQS_CLK and DQSN_CLK) from a clock signal (DQS)

which is input to said clock input terminal (column 2, lines 37-62); and a latch circuit (21 and

22) for latching a data signal input (DQ) to said data input terminal synchronously with said

internal clock signal (Coteus discloses the incoming data being input into latches [21 and 22] are

synchronized with the internal clocks [DQS_CLK and DQSN_CLK] as latch enable signals

15   CLKS; column 2, lines 54-62).

Coteus fails to disclose said internal clock generating circuit includes: a variable delay

circuit for receiving said clock signal and outputting said internal clock signal; a dummy variable

delay circuit for delaying an output signal of said variable delay circuit; a first frequency divider

for dividing frequency of an output signal of said dummy variable delay circuit; a second

20   frequency divider for dividing frequency of said clock signal or the inversion signal of said clock

signal; a phase comparator for comparing phase of a first frequency divided signal output from

the first frequency divider with phase of a second frequency divided signal output from the

second frequency divider; and a delay control circuit for outputting a delay control signal for

controlling said variable delay circuit and said dummy variable delay circuit on the basis of an

output signal of said phase comparator, wherein said first frequency divider generates a first

frequency divided signal synchronized with the (i-j)th switch timing of said clock signal (where i

5   denotes an integer of 1 or larger and j denotes an integer of 0 or larger), wherein said second

frequency divider generates a second frequency divided signal synchronized with the (i+1+j)th

switch timing of said clock signal, wherein said phase comparator compares the phase of said

first frequency divided signal with the phase of said second frequency divided signal to obtain a

phase difference, and wherein said delay control circuit controls delay times of said variable

10   delay circuit and said dummy variable delay circuit so that said phase difference becomes zero.

        Kawasaki teaches said internal clock generating circuit includes: a variable delay circuit

(12) for receiving said clock signal (i-clk) and outputting said internal clock signal (dll-clk)

(column 6, lines 37-41); a dummy variable delay circuit (21) for delaying an output signal of said

variable delay circuit (Kawasaki discloses the dummy delay circuit 21 indirectly receiving the

15   signal from the variable delay circuit 12 via clock selection circuit 30, frequency divider 16 and

second variable delay circuit 19; column 6, line 57 thru column 7, line 8 and column 7, line 63

thru column 8, line 9); a first frequency divider (32) for dividing frequency of an output signal

(dll-clk) of said variable delay circuit (12) (column 8, lines 50-59); a second frequency divider

(31) for dividing frequency of said clock signal (i-clk) or the inversion signal of said clock signal

20   (column 8, lines 50-59); a phase comparator (33) for comparing phase of a first frequency

divided signal (dll-clk-div) output from the first frequency divider (32) with phase of a second

frequency divided signal (i-clk-div) output from the second frequency divider (32) (column 8,

lines 60-67); and a delay control circuit (18) for outputting a delay control signal for controlling

said variable delay circuit (12) and said dummy variable delay circuit (21 via additional variable

delay circuit; column 6, line 57 thru column 7, line 8) on the basis of an output signal (CKS) of

said phase comparator (33) (Kawasaki discloses the output signal [CKS] from the phase

5   comparator [33] indirectly controls, via a second phase comparator [17], the control signal from

the delay control circuit [18] for delay circuit 12 and dummy delay circuit 21 indirectly by

controlling the frequency divider 16 which supplies d-dll-clk to dummy signal; column 7, lines

9-17 and column 7, lines 31-55). Kawasaki also has the added feature of reducing excessive

power consumption and shorten a time period required for achieving a lock-on condition when a

10   clock signal switches from a longer cycle to a shorter cycle (column 3, lines 50-55).

        It would have been obvious to one of ordinary skill of the art having the teachings of

Coteus and Kawasaki at the time the invention was made, to modify the clock generation circuit

of Coteus to include the DLL components as taught by Kawasaki such that said first frequency

divider generates a first frequency divided signal synchronized with the (i-j)th switch timing of

15   said clock signal (where i denotes an integer of 1 or larger and j denotes an integer of 0 or larger)

and said second frequency divider generates a second frequency divided signal synchronized

with the (i+1+j)th switch timing of said clock signal. One of ordinary skill in the art would be

motivated to make this combination altering the clock generating circuit to include the DLL

componenets in view of the teachings of Kawasaki, as doing so would give the added benefit of

20   reducing excessive power consumption and shorten a time period required for achieving a lock-

on condition when a clock signal switches from a longer cycle to a shorter cycle (column 3, lines

50-55).

Neither Coteus nor Kawasaki teaches the phase comparator compares the phase of said

first frequency divided signal with the phase of said second frequency divided signal to obtain a

phase difference or the delay control circuit controls delay times of said variable delay circuit

and said dummy variable delay circuit so that said phase difference becomes zero.

5   Fujieda teaches another internal semiconductor DLL that comprises three variable delay

circuits (41, 42 and 45) that all have the same configuration and are all controlled by the delay

control circuit (47) (column 6, lines 10-16 and column 9, lines 16-24). Fujieda further teaches a

phase comparator (44) that measures the phase difference between two different divided clock

signals (X and Z), delivers a resultant phase difference signal to the delay control circuit (47) to

10   ensure that the variable delay times of the first, second and third variable delay signals have a

zero phase difference (column 5, line 61 thru column 6, line 10). Fujieda also has the added

feature of providing the semiconductor device does not cause an underflow and an overflow of a

DLL circuit even if the frequency of the internal clock becomes high or low (column 2, lines 35-

41).

15   It would have been obvious to one of ordinary skill of the art having the teachings of

Coteus, Kawasaki and Fujieda at the time the invention was made, to modify the clock

generating circuit of Coteus and Kawasaki to include the addition features as taught by Fujieda

such that the third delay circuit is a variable delay circuit wherein said third delay circuit also has

the same configuration as the first and second variable delay circuits and the phase comparator

20   obtaining a phase difference and that said delay control circuit controls delays of the first, second

and third variable circuits so that said phase difference becomes zero. One of ordinary skill in the

art would be motivated to make this combination of including the additional DLL features in

view of the teachings of Fujieda, as doing so would give the added feature of providing the

semiconductor device does not cause an underflow and an overflow of a DLL circuit even if the

frequency of the internal clock becomes high or low (column 2, lines 35-41).

As to claim 10, Coteus discloses the semiconductor integrated circuit further comprising

5   a memory cell array in which a plurality of memory cells are arranged in an array, wherein write

data to any of said memory cells can be transmitted as said data signal to said latch circuit

(Coteus discloses the clock generation circuit being used within a SDRAM-DDR which, as is

known in the art, comprises arrays of memory cells and writing and reading sigals; column 1,

lines 12-22).

10

Conclusion

Any inquiry concerning this communication or earlier communications from the

15   examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The

examiner can normally be reached on 8AM - 4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the

organization where this application or proceeding is assigned is (571) 273-8300.

20   Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free).

James F. Sugent
5   Patent Examiner, Art Unit 2116
May 19, 2006

THUAN N. DU
PRIMARY EXAMINER